Simple Model for Dynamic Range Estimate of GaAs Amplifiers

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ABSTRACT — **The method to estimate the dynamic range of low bias power low noise GaAs amplifiers for portable radio communication equipment is presented. The method uses the extension of a simple linear noise model of the microwave FET, major components of which are bias dependent. Both noise figure and intermodulation distortion of an amplifier may be predicted with this model and the dynamic range is easily calculated as a function of bias current and transistor width. The model unifies small signal and nonlinear properties in a form suitable for manual computation.**

I. Introduction

Intermodulation distortion (IMD) should be minimized in practically all receiver circuits to enhance their functionality. Many publications are devoted to the problem of modeling the IMD properties of microwave amplifiers. In this work the emphasis is put on the low bias power, low noise amplifiers operating in lower microwave bands (< 3 GHz).

The bias dependent noise model of the microwave FET (MESFET or HEMT) – used in this work - has been presented in detail before [1][2]. This model is applied here to the computation of the IMD in amplifiers operating at lower microwave frequencies, when nonlinear capacitance effects may be neglected. The key components of the model in this respect are: the transconductance g_m and the drain-source conductance $g_{ds.}$ - both are the function of the DC drain current I_D. The model also makes possible the evaluation of the noise figure of an amplifier – thus the dynamic range may be determined.

II. Bias Dependent GaAs FET Model

The dependence of g_m and g_{ds} on the I_D has been modeled with simple functions given in (1)

$$g_m(I_D) = g_{mo}\frac{(1+a+b)x^2}{x^2+ax+b}$$
$$g_{ds}(I_D) = g_{dso}\frac{(1+c+d)x^2}{x^2+cx+d} \quad (1)$$

where:

$x = I_D / I_{dss}$ - the ratio of the drain current to the current at zero gate voltage

g_{mo}, g_{dso} - the value of a parameter for the drain current $I_D = I_{dss}$, i.e. $x = 1$.

a, b, c, d – are model parameters. Usually $a \approx c$, $b \approx d$ – this approximation will be used later.

Parameters: g_{mo}, g_{dso} are proportional to the gate width w and, for a given technological process may be expressed as: $g_{mo} = w \times g_{mpo}$, $g_{dso} = w \times g_{dpo}$ - where g_{mpo} , g_{dpo} are conductances per mm of gate width and are characteristic of the process.

This model has been verified [2] for a number of transistors manufactured in the Philips ED02AH process and was accurate to a few percent over the x parameter range of 0.005 to 1.

The noise factor F of a transistor as a function of source impedance $Z_s = R_s + jX_s$ is predicted with this model [1] as

$$F = 1+\frac{qC_nI_D}{2kT_og_m^2}\omega^2C_{gs}^2(R_s+R_g+R_c)^2+\frac{R_c}{R_s}+\frac{R_g}{R_s} \quad (2)$$

if the reactance at the input is tuned out (i.e. $X_x = X_{sopt}$). R_g is the gate metal resistance, R_c – resistance of the portion of the channel under the gate and C_n is the dimensionless model parameter (typ. $C_n \approx 0.255$ for the ED02AH process). While the g_m parameter is a function of the drain current, the optimum I_D value may be found analytically and is given by $x_{opt} = (a+\sqrt{a^2+12b})/2$.

III. Intermodulation Distortion In A Single Stage Amplifier

At lower microwave frequencies (up to approx. 3 - 4GHz) the operation of GaAs MESFET and HEMT transistors is little affected by transistor capacitances under normal operating conditions. Usually the transistor is severely mismatched at the input because of stability or noise optimization reasons. The device may be regarded as 'voltage controlled' which results in little influence of the nonlinearity of the gate source capacitance C_{gs} and the feedback capacitance C_{gd}. For the estimate of the distortion a quasi-static approach, which neglects these effects, was adopted.

A. Common Source Amplifier

With the assumption of small amplitudes of interfering signals the derivation of the output current into the load

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may be based on differential parameter changes. The geometrical construction to compute the current I_L into the load is shown in Fig. 1.

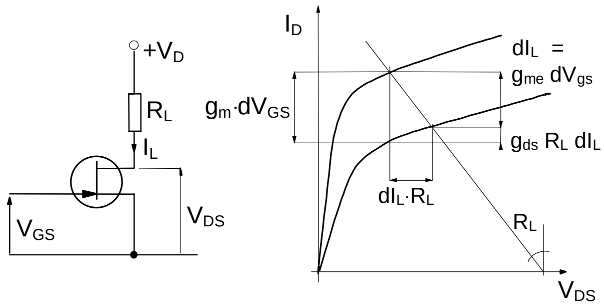

Fig. 1. Geometric derivation of load current vs. V_{GS} change

AC component of the load current I_L in response to the gate control voltage $V_{gsi} = dV_{GS}$ is equal (assuming $a = c$, $b = d$)

$$g_{me}(I_D) = \frac{dI_L}{dV_{GS}} = \frac{g_m(I_D)}{1 + g_{ds}(I_D)R_L} \approx$$
$$\approx \frac{g_{mo}(1+a+b)x^2}{x^2 + ax + b + g_{dso}x^2(1+a+b)R_L} \qquad (3)$$

The same result may obviously be achieved with the equivalent small signal model – the figure was used here to explicitly show the dependence on both drain current and drain voltage changes.

Equation (3) will be used to compute the derivatives of the 'effective' transconductance g_{me} vs. gate voltage. V_{gsi} may be different from the input voltage to the stage V_{in}, when significant source feedback impedance Z_{sf} exists. In this case V_{gsi} may be taken as a portion of V_{in}

$$V_{gsi} \cong \frac{V_{in}}{1 + g_m Z_{sf}} \qquad (4)$$

Original formulae (1) form the functions of the drain current I_D through the variable x. The derivatives vs. V_{GS} will be determined from the inverse function (5)

$$dV_{GS} = \frac{\left[1 + g_{dso}R_L(1+a+b) + \frac{a}{x} + \frac{b}{x^2}\right]}{g_{mo}(1+a+b)} dI_o =$$
$$= F\left(G + \frac{a}{x} + \frac{b}{x^2}\right)dI_o \qquad (5)$$

where $F = 1/g_{mo}(1 + a + b)$, $G = 1 + g_{dso}R_L(1 + a + b)$

The derivatives vs. I_L are given in (6) and the required derivatives versus V_{GS} are given by (7).

$$\frac{dV_{GS}}{dI_o} = r_{me} = \frac{F}{I_{dss}}\left(G + \frac{a}{x} + \frac{b}{x^2}\right)$$
$$\frac{d^2V_{GS}}{dI_o^2} = r'_{me} = \frac{F}{I_{dss}^3}\left(-\frac{a}{x^2} - \frac{2b}{x^3}\right) \qquad (6)$$
$$\frac{d^3V_{GS}}{dI_o^3} = r''_{me} = \frac{F}{I_{dss}^3}\left(\frac{2a}{x^3} + \frac{6b}{x^4}\right)$$

$$g'_{me} = \frac{d^2I_L}{dV_{GS}^2} = -\frac{r'_{me}}{r_{me}^3}$$
$$g''_{me} = \frac{d^3I_L}{dV_{GS}^3} = -\frac{r''_{me}\cdot r_{me} - 3(r'_{me})^2}{r_{me}^5} \qquad (7)$$

The plots of derivatives vs. drain current typical for the ED02AH process are shown in Fig. 2 and 3.

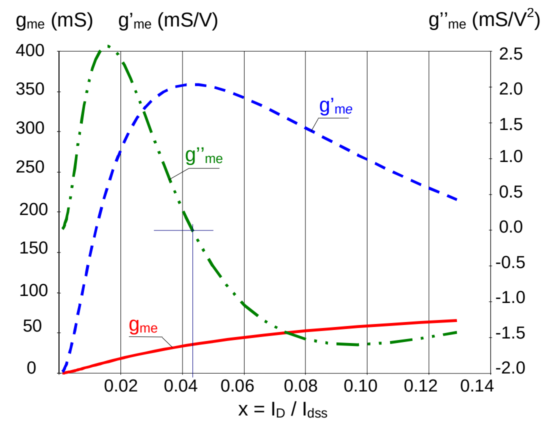

Fig. 2. Derivatives of drain current (I_L) vs. normalized drain current. R_L = 50 Ω

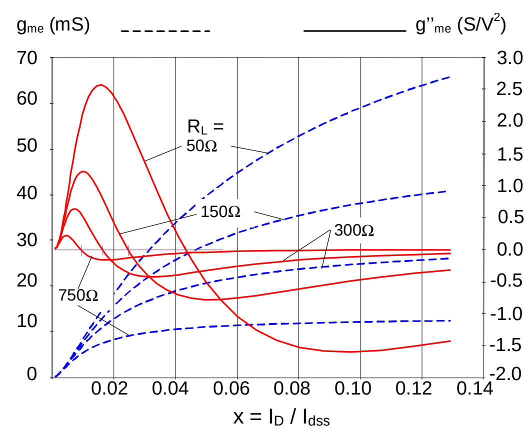

Fig. 3. Transconductance g_{me} and its second derivative vs. x for various load resistances

The parameters for Fig. 2 and 3 – typical of the Philips process are as follows: I_{dss} = 80 mA, g_{mpo} = 0.51696 S, g_{dpo} = 0.04189 S, a = 0.14616, b = 0.000799 for the gate width w = 400 µm, V_{DS} = 2 V.

The shape of the curves in these figures corresponds well to the data presented in other publications [3][4]. The cancellation of the third order IMD is possible at certain value of the drain current. What is important is that the cancellation point depends on the actual load resistance and shifts toward lower current with the increase in R_L. This phenomenon is the result of the g_{ds} nonlinearity which acts in the opposite direction than the g_m nonlinearity.

Under large signal operation the AC component of the current I_L delivered into the load may be expressed by this series expansion

$$I_L(V_{gsi}) = g_{me}V_{gsi} + \frac{1}{2}g'_{me}V_{gsi}^2 + \frac{1}{6}g''_{me}V_{gsi}^3 + \ldots \quad (8)$$

For the third order intermodulation test the control voltage V_{gsi} may be of the form

$$V_{gsi}(t) = V_m\cos(\omega_1 t) + V_m\cos(\omega_2 t) \quad (9)$$

and the amplitudes of the output current components of interest are

$$\begin{aligned} I_o(\omega_1) = I_o(\omega_2) &= g_{me}V_m + \frac{9}{24}g''_{me}V_m^3 \\ I_o(2\omega_1-\omega_2) = I_o(2\omega_2-\omega_1) &= \frac{1}{8}g''_{me}V_m^3 \end{aligned} \quad (10)$$

A practical measure of the third order intermodulation distortion at a given signal level is the ratio of amplitudes of the load current at fundamental frequency (ω_1 or ω_2) and one of the IM product frequencies ($2\omega_1 - \omega_2$ or $2\omega_2 - \omega_1$), and its inverse is given by (11).

$$(d_{IM3})^{-1} = \frac{I_o(\omega_1)}{I_o(2\omega_1-\omega_2)} = \frac{8}{V_m^2}\cdot\left|\frac{g_{me}(I_D)}{g''_{me}(I_D)}\right| + 3 \quad (11)$$

After the derivatives (6) and (7) are substituted into equation (11) the expression for d_{IM3} becomes

$$(d_{IM3})^{-1} = \\ = \frac{8}{V_m^2}\frac{I_{dss}^2}{g_{mo}^2}\cdot\left|\frac{(Gx^2+ax+b)^4(1+a+b)^{-2}x^{-2}}{2aGx^2 - a^2x^2 - 4abx + 6bGx^2 - 6b^2}\right| + 3 \quad (12)$$

The ratio I_{dss}/g_{mo} is characteristic of a given process and does not change with the FET width.

B. Cascode Amplifier

For the cascode amplifier shown in Fig. 4, the 'equivalent' transconductance g_{me} similar to (3) may be computed, when the current through the second transistor C_{gs} capacitance is neglected. In this case the current I_L is equal to the first stage output current I_{o1} and thus the second transistor does not introduce distortion except for presenting nonlinear load Z_{iss} to the first transistor.

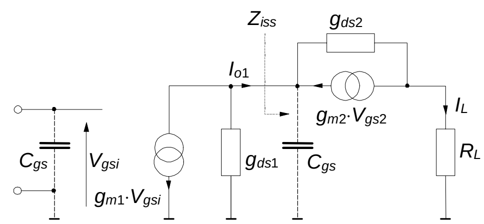

Fig. 4. Equivalent circuit for the cascode amplifier in the low frequency range

With Z_{iss} given by (13) below

$$Z_{iss} = \frac{1+g_{ds}R_L}{g_m + g_{ds}} \quad (13)$$

the equivalent transconductance g_{me} is equal to

$$g_{me} = \frac{g_{mo}x^2}{E\left(Gx^2+ax+b\right)} \quad (14)$$

where $E = \frac{1+2A}{1+A}\cdot\frac{1}{1+a+b}$ $\quad A = \frac{g_{dso}}{g_{mo}}$ $\quad G = 1 + \frac{A^2 g_{mo}R_L}{(1+A)E}$

Required derivatives and the IMD level are computed as before. With the knowledge of the input circuit structure the amplitude of V_{gsi} for a given signal power may be computed and subsequently the distortion ratio d_{IM3} and the noise figure /from (3)/.

IV. Experimental Results

Two MMIC amplifiers have been built in the ED02AH technology. The designed center frequency for both was 2.4 GHz. A single transistor circuit is shown in Fig. 5.

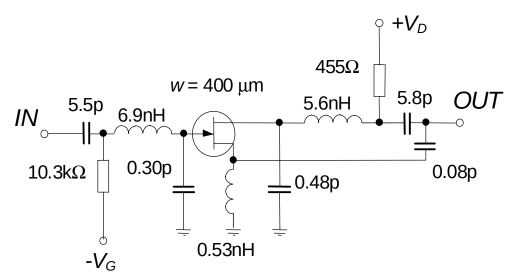

Fig. 5. Simplified schematics of a single transistor common source amplifier

Theoretical parameters shown in Fig. 6 were computed for the gate voltage V_m = 17 mVp per tone and the noise figure in Fig. 9 for the source resistance R_s = 135 Ω.

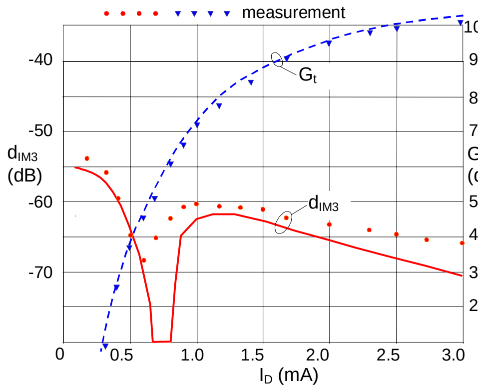

Fig. 6. Measured gain and intermodulation distortion (points) vs. predicted parameters (lines). P_{in} = -35 dBm/tone, f_1 = 2.40 GHz, f_2 = 2.402 GHz

The cascode amplifier (Fig. 7) was slightly mistuned and the measurements presented were performed at f = 2.6 GHz. Source resistance for the computation of NF was 175 Ω

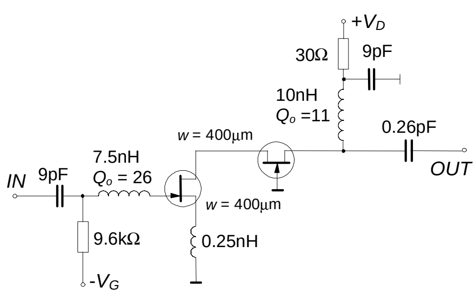

Fig. 7. Approximate schematics of a cascode amplifier

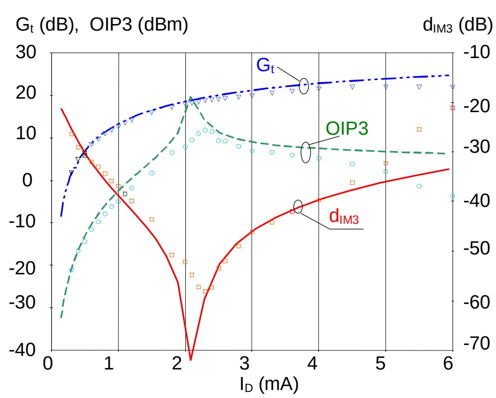

Fig. 8. Measured gain and intermodulation parameters (points) vs. results for model (lines). P_{in} = -36 dBm/tone, f_1 = 2.60 GHz, f_2 = 2.602 GHz

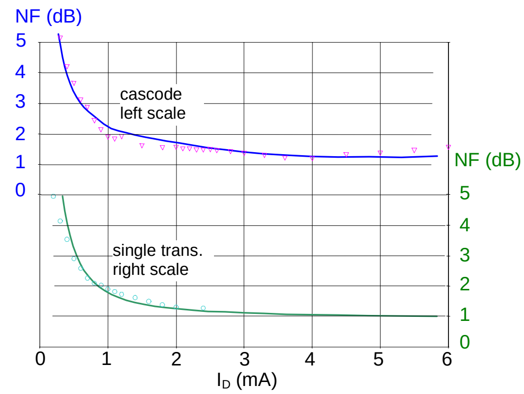

Fig. 9. Measured (points) and computed (lines) noise figure for both amplifiers as a function of the drain current

V. Conclusion

The model presented here is capable of predicting the intermodulation distortion and noise figure of low bias power amplifiers. The accuracy is quite good at lower microwave frequencies although the model is derived from a linear description of a GaAs transistor. Simple formulae permit quick evaluation of amplifier properties and may help optimize transistor geometry.

For very low bias currents investigated here a single transistor amplifier provides lower distortion at comparable bias power. For higher currents a cascode circuit is better.

Acknowledgement

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